

PATENT

IN THE UNITED STATES PATENT OFFICE

Applicant: Robert Yin et al.
Assignee: Xilinx, Inc.
Title: "Method and System for Controlling Default Values
of Flip-Flops in PGA/ASIC-Based Designs"

Serial No.: 10/082,630 File Date: February 22, 2002
Examiner: Unknown Art Unit: 2819
Docket No.: X-1070 US Conf. No.: 4447

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

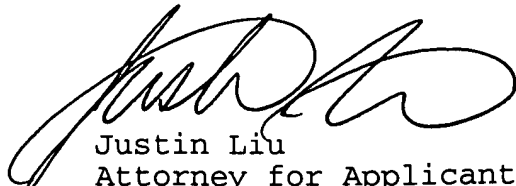
Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the One Hundred Seven (107) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

These references were cited in related U.S. patent applications. This Information Disclosure Statement is being filed under 37 CFR 1.97(b) prior to the receipt of a first office action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

Respectfully submitted,


Justin Liu
Attorney for Applicants
Reg. No. 51,959

I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, Virginia, 22313-1450 on January 16, 2004.

Julie Matthews
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if Known	
				Application / C nf. N .	10/082,630 / 4447
				Filing Dat	February 22, 2002
				First Named Invent r	Robert Yin
				Art Unit	2819
				Examiner Name	Unknown
				Attorney Docket Number	X-1070 US
Sheet	1	of	7		

U.S. PATENT DOCUMENTS					
Examiner Initials *	Cite No.†	Document Number Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 4,758,985	07-19-88	Carter	
		US- 5,142,625	08-25-92	Nakai	
		US- 4,855,669	08-08-89	Mahoney	
		US- 34,363	08-31-93	Freeman	
		US- 5,072,418	12-10-91	Boutaud et al.	
		US- 5,274,570	12-28-93	Izumi et al.	
		US- 5,550,782	08-27-96	Cliff et al.	
		US- 5,347,181	09-13-94	Ashby et al.	
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		US- 5,311,114	05-10-94	Sambamurthy et al.	
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		US- 5,552,722	09-03-96	Kean	
		US- 6,467,009	10-15-02	Winegarden et al.	
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		US- 5,457,410	10-10-95	Ting	
		US- 5,740,404	04-14-98	Baji	
		US- 5,581,745	12-03-96	Muraoka	
		US- 5,742,179	04-21-98	Sasaki	
		US- 5,600,845	02-04-97	Gilson	
		US- 5,574,930	11-12-96	Halverson Jr., et al.	

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Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Sheet 2 of 7

Complete if Known

Application / Conf. N .	10/082,630 / 4447
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First Named Inventor	Robert Yin
Art Unit	2819
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Attorney Docket Number	X-1070 US

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OTHER - NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	/	SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	/	VASON P. SRINI, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	/	G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	/	JACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	/	CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	/	P.C. FRENCH et al., "A SELF-RECONFIGURING PROCESSOR," IEEE, July 1993, pp. 50-59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	/	Christian Iseli et al., "SPYDER: A RECONFIGURABLE VLIW PROCESSOR USING FPGA's," IEEE, July 1993, pp. 17-24, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	/	MICHAEL I. WIRTHLIN et al., "THE NANO PROCESSOR: A LOW RESOURCE RECONFIGURABLE PROCESSOR," IEEE, February 1994, pp. 23-30, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	/	WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	/	ANDRE' DEHON, "DPGA-COUPLED MICROPROCESSORS: COMMODITY ICs FOR THE EARLY 21ST CENTURY," IEEE, February 1994, pp. 31 - 39, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	/	OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

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Sheet	3	of	7
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Complete if Known

Applicati n / C nf. No.	10/082,630	/	4447
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Filing Dat	February 22, 2002
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First Named Inventor	Robert Yin
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Art Unit	2819
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Examiner Name	Unknown
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Attorney Docket Number	X-1070 US
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Examiner Initials *	Cite No.¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 5,473,267	12-05-95	Stansfield	
		US- 5,742,180	04-21-98	DeHon et al.	
		US- 5,737,631	04-07-98	Trimberger	
		US- 5,748,979	05-05-98	Trimberger	RECEIVED
		US- 6,578,174	06-10-03	Zizzo	
		US- 6,026,481	02-15-00	New et al.	JAN 22 2004
		US- 5,705,938	01-06-98	Kean	
		US- 5,500,943	03-19-96	Ho et al.	Technology Center 2100
		US- 6,483,342	11-19-02	Britton et al.	
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		US- 5,543,640	08-06-96	Sutherland et al.	
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		US- 5,874,834	02-23-99	New	
		US- 5,835,405	11-10-98	Tsui et al.	

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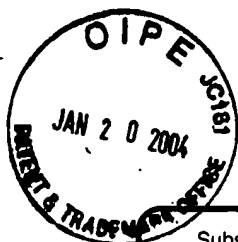
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Sheet 4 of 7

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Filing Date	February 22, 2002
First Named Inventor	Robert Yin
Art Unit	2819
Examiner Name	Unknown
Attorney Docket Number	X-1070 US

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OTHER - NON PATENT LITERATURE DOCUMENTS

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Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	✓	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
	✓	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
	✓	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-9 to 2-18; 2-187 to 2-199, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
	✓	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-107 to 2-108, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
	✓	CHRISTIAN ISELI et al., "AC++ COMPILER FOR FPGA CUSTOM EXECUTION UNITS SYNTHESIS," 1995, pp. 173-179, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	✓	INTERNATIONAL BUSINESS MACHINES, "POWERPC 405 EMBEDDED PROCESSOR CORE USER MANUAL," 1996, 5TH Ed., pp. 1-1 TO X-16, International Business Machines, 1580 Rout 52, Bldg. 504, Hopewell Junction, NY 12533-6531.	
	✓	YAMIN LI et al., "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	✓	RALPH D. WITTIG et al., "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC, April 17, 1996, pp 126-135, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	✓	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
	✓	WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
	✓	XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

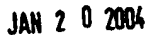
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Filing Date	February 22, 2002
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First Name of Inventor	Robert Yin
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Art Unit	2819
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Examiner Name	Unknown
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Attorney Docket Number	X-1070 US
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		US- 6,519,753	02-11-03	Ang	
		US- 6,434,735	08-13-02	Watkins	
		US- 6,588,006	07-01-03	Watkins	
		US- 6,539,508	03-25-03	Patrie et al.	
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		US- 6,353,331	03-05-02	Shimanek	
		US- 6,507,942	01-14-03	Calderone et al.	
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		US- 6,611,951	08-26-03	Tetelbaum et al.	
		US- 6,522,167	02-18-03	Ansari et al.	
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		US- 6,541,991	04-01-03	Horncheck et al.	
		US- 09/858,732	05-15-01	Schulz	
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		US- 6,601,227	07-29-03	Trimberger	
		US- 09/917,304	07-27-01	Douglass et al.	
		US-			
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FOREIGN PATENT DOCUMENTS

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